REMARKS

With the above amendments, claims 1, 5-11, and 15-21 remain in the application. Claims 1, 5, 7, 8, 11, 15, 17, 18, and 21 have been amended. No new matter is being added.

Claim Rejections 35 U.S.C. § 103

The claims stand rejected as unpatentable over Swanberg et al. (USP 6,895,508) in view of Draves et al (USP 5,950,221). Applicants respectfully traverse this rejection with respect to the claims as hereby amended.

Claim 1 is hereby amended and now recites as follows.

> 1.   A memory system for a computer, the memory system comprising **a single memory page including a kernel stack, a register stack engine (RSE) stack, and a data structure comprising system information about a user process**, the kernel stack being separate and distinct from user program stacks in the memory system, wherein **the kernel stack and the RSE stack are separated by said data structure**, and wherein **the kernel stack and the RSE stack are configured to grow apart in opposite directions away from said data structure**.

(Emphasis added.)

As seen above, amended claim 1 now requires that a **single** memory page includes at least **three elements**, namely the kernel stack, the RSE stack and the **data structure comprising system information about a user process.** Moreover, claim 1 now requires that **the kernel stack and the RSE stack are**

separated by said data structure. Furthermore, claim 1 now also recites that the **"the kernel stack and the RSE stack are configured to grow apart in opposite directions away from said data structure."** These limitations are incorporated into claim 1 from dependent claims 2-4.

These limitations are described in the originally-filed application, for example, in relation to FIG. 4, which is reproduced below for convenience. The Uarea 406 in FIG. 4 corresponds to the data structure comprising system information about a user process.
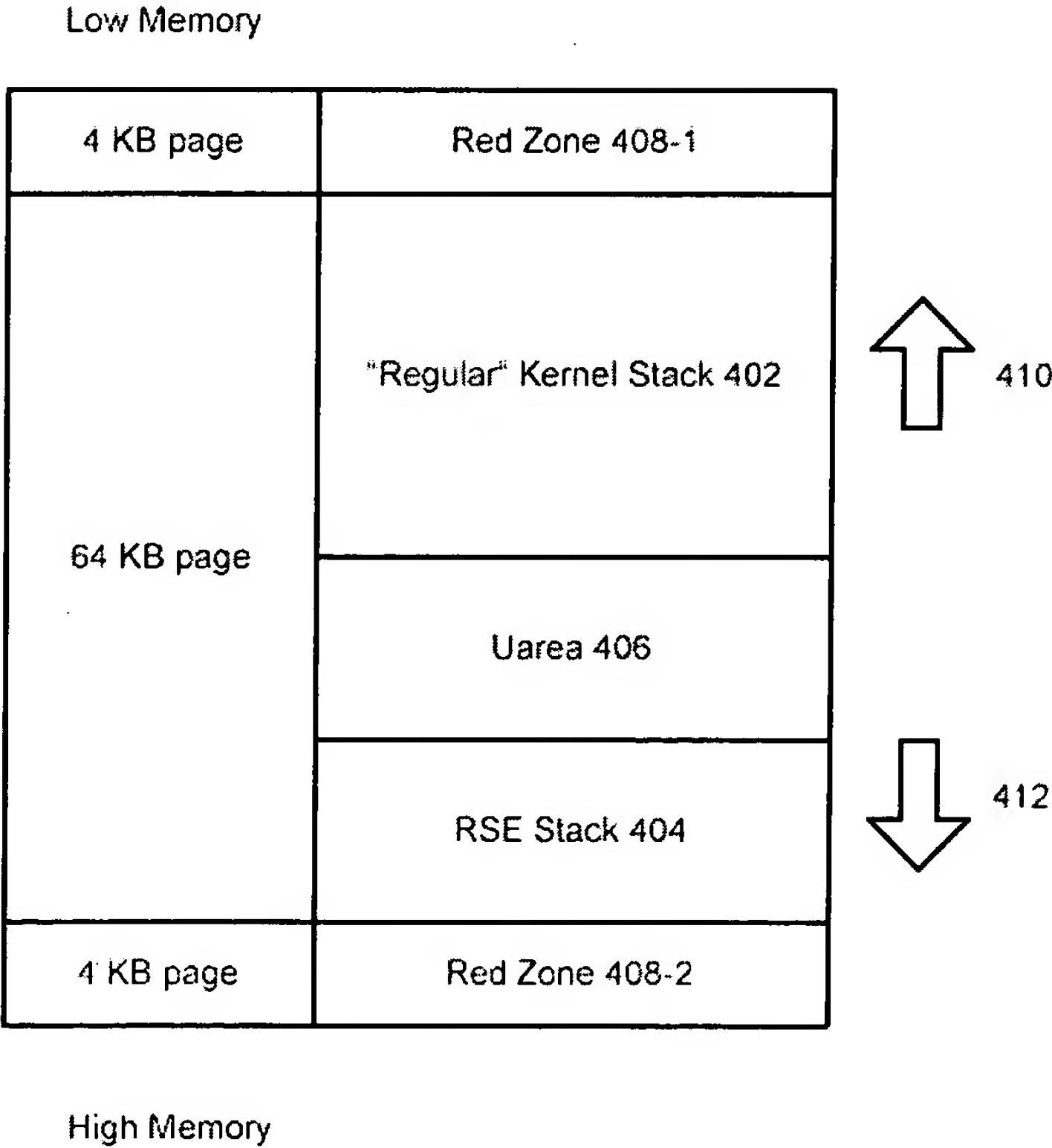
Low Memory

4 KB page	Red Zone 408-1
64 KB page	"Regular" Kernel Stack 402
	Uarea 406
	RSE Stack 404
4 KB page	Red Zone 408-2

410

412

High Memory

FIG. 4

Advantages of the claimed memory system are described, for example, on page 7, lines 18-24 of the original application. The claimed memory system advantageously provides for higher performance by reducing the number of translation lookaside buffer (TLB) misses that typically occur as a new process enters the kernel. Dependent claim 7 relates to this reduction in TLB misses and recites that "the number of translation lookaside buffer (TLB) misses when a process 'enters' a kernel ... is no more than one TLB miss." In addition, the claimed memory system architecture advantageously facilitates implementation of dynamic growth of the "regular" kernel stack and the RSE stack over time.

In contrast, Swanberg et al. discloses Register Stacks 403 and Memory Stacks (user program stacks) 402 as **immediately adjacent to each other, without any data structure therebetween**. This is shown in FIG. 4B of Swanberg et al., which is reproduced below for convenience.
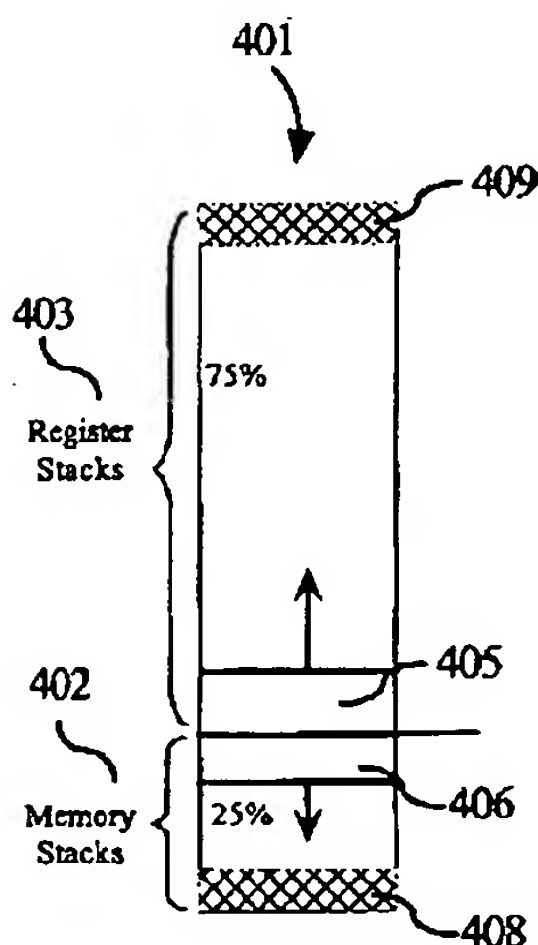

FIG. 4B
PRIOR ART

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Note from FIG. 4B (and the description in column 3) that element 405 in Swanberg et al. represents the dynamically-assigned addresses of the register stack 403 and is **not** a structure separate from the register stack 403. Hence, **element 405 cannot comprise the claimed data structure**. Similarly, element 406 in Swanberg et al. represents the dynamically-assigned addresses of the memory stacks 402 and is **not** a structure separate from the memory stacks 402. Hence, **element 406 cannot comprise the claimed data structure.**

Furthermore, as discussed in the prior response to office action, **the memory stacks 402** of Swanberg et al. are user program stacks which **cannot** be **the claimed kernel stack**.

For at least the above-recited reasons, Swanberg et al. does not disclose or teach the claimed memory system as recited in claim 1.

Draves et al. is cited for disclosing that the kernel stack is separate and distinct from user program stacks in a memory system. Hence, the citation to Draves et al. does **not** disclose or teach the claimed memory system as recited in claim 1.

For at least the above-discussed reasons, applicants respectfully submit that claim 1, as amended hereby, is now patentably distinguished over the cited references.

Claims 5-10 depend from claim 1. As such, applicants respectfully submit that claims 5-10 are now also patentably distinguished over the cited art for at least the reasons discussed above in relation to claim 1.

Similarly, claim 11 is hereby amended and now also requires that the single memory page includes, in addition to the kernel stack and the RSE stack, "a **data structure** comprising system information about a user process". Claim 11 also

requires the kernel stack and the RSE stack to be "**separated by** said data structure," and that "the **kernel** stack and the RSE stack are configured to **grow apart in opposite directions away from said data structure**."

Hence, for at least the same reasons discussed above in relation to claim 1, claim 11 as amended is now also patentably distinguished over the cited art.

Claims 15-20 depend from claim 11. As such, applicants respectfully submit that claims 15-20 are now also patentably distinguished over the cited art for at least the reasons discussed above in relation to claim 11.

Similarly, claim 21 is hereby amended and now also requires that the single memory page includes, in addition to the kernel stack and the RSE stack, "a **data structure** ... wherein said data structure comprises system information about a user process". Claim 21 also requires that "the **kernel** stack and the RSE stack **are configured to grow apart in opposite directions away from said data structure**."

Hence, for at least the same reasons discussed above in relation to claim 1, claim 21 as amended is now also patentably distinguished over the cited art.
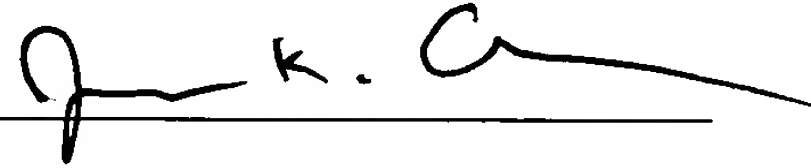
Conclusion

For at least the above reasons, it is respectfully submitted that claims 1, 5-11, and 15-21 are now patentably distinguished over the cited art. The Examiner is invited to telephone the undersigned at (408) 436-2111 for any questions.
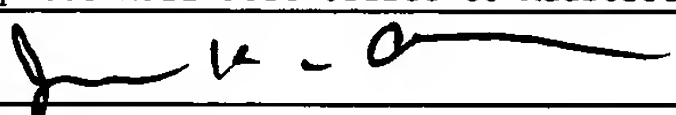
If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 08-2025.

Respectfully submitted,
Christopher Philip Ruemmler, et al.

Dated: _____ May 9, 2006 _____

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